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09/771,229	01/26/2001	Takanori Iwamatsu	FUJS 13.045A	6938

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EXAMINER	
TSE, YOUNG TOI	

ART UNIT	PAPER NUMBER
2637	16

DATE MAILED: 07/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/771,229	Applicant(s) IWAMATSU ET AL.	
	Examiner YOUNG T. TSE	Art Unit 2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Reissue Applications

Response to Arguments

1. Applicant's arguments filed 26 August 2003 have been fully considered but they are not persuasive.

2. With respect to claim 47, Applicants argue that both Onoda and Kobayashi fail to disclose that detection unit or detector circuit(s) detects either of difference information between the demodulated signal and the equalized demodulated signal or a combination of clock phase difference information and signal error differential information.

3. The examiner does not agree with applicant's arguments. In Figure 5 of Onoda patent, the phase detection unit 2 detects the phase difference between the outputs X and Y of the A/D converters 57 and 58 and the output (d) of the digital PLL 3. Wherein the output (a) is the in-phase channel outputted from the A/D converter 57 through the operation circuit 59 for generating signal error differential information and the clock signal (d) for generating clock phase difference information and is provided by the divider 34 of the digital PLL 3. The digital PLL 3 also provides a clock signal (b) to the A/D converters 57 and 58 through the divider 33 having the frequency twice of the frequency of the clock signal (d).

4. For the similar arguments set forth described above.. In Figure 2 of Kobayashi's patent, the detector circuits 43, 45, 46 and 47 detect the phase difference between the outputs c and d of the A/D converters 41 and 42 and the output m of the clock

reproducer 48. Wherein the A/D converters 41 and 42 generate signal error differential information and the clock reproducer 48 provides clock phase difference information to the phase detector circuits 45, 46 and 47. The clock producer 48 also provides a clock signal m to the A/D converters 41 and 42 and the delay detector 43. Figure 12 shows a similar circuitry of Figure 2, however, the clock reproducer 48 generates a common clock signal to the A/D converters 41 and 42 and the phase error detector 47a. Therefore, claim 47 is unpatentable over Onoda and Kobayashi.

5. The reissue oath/declaration filed with this application is defective (see 37 CFR 1.175 and MPEP § 1414) because of the following:

6. As pointed out in the last Office Action, Applicants are requested to submit a new oath or declaration to correct the errors why to change the preamble of claims 1-14, the newly added claim 47, the changes in the claims, the specification, the drawing and the amended claims 8, 14 and the cancelled claims 15-46 filed on 26 August 2003.

7. Claims 1-14 and 47 are rejected as being based upon a defective reissue declaration under 35 U.S.C. 251 as set forth above. See 37 CFR 1.175.

The nature of the defect(s) in the declaration is set forth in the discussion above in this Office action.

Drawings

8. The drawings were received on 26 August 2003. These drawings are acceptable.

Specification

9. The disclosure is objected to because of the following informalities: column 14, line 1, "14" should be changed to –14A – (also see last Office Action). Appropriate correction is required.

Claim Objections

10. Claims 3-28, 30-32, 34-39, and 41-46 are objected to because of the following informalities: in claim 1, line 10, "said clock" should be – said signal identification clock --; in claim 2, line 10, "said clock" should be – said signal identification clock --; in claim 5, line 12, "said identifying units" should be – said plural identifying units --; in claim 8, line 7, "said clock" should be – said signal identification clock – and line 16, "is said" should be – of said --; in claim 11, line 12, "said identifying units" should be – said plural identifying units --; and in claim 47, line 17, "phase information" should be – phase difference information --, line 19, "information" should be – differential information --, line 27, "of clock phase" should be – of the clock phase – and line 28, "and signal error" should be – and the signal error --. Appropriate correction is required.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

12. Claim 47 is rejected under 35 U.S.C. 102(b) as being anticipated by Onoda et al.

13. Onoda et al. (U.S. Patent No. 5,317,602) discloses an orthogonal or QPSK receiver in Fig. 5 including mixers 51 and 52 for mixing an IF signal with a local oscillator signal generated by a local oscillator 53; filters 55 and 56 for filtering the mixed signals; A/D converters 57 and 58 for converting the filtered signals into digital signals; an operation circuit 59, and discriminators 60 and 61 for converting the digital signals into an in-phase (I) signal and a quadrature-phase (Q) signal; a P/S converter 62 for converting the quadrature signals into a serial signal; and a bit time recovery circuit 1 for providing clock signals to the A/D converters 57 and 58, the operation circuit 59, the discriminators 60 and 61, and the P/S converter 62.

The bit time recovery circuit 1 includes a phase comparison result detection unit 2 and a digital PLL unit 3. The phase comparison result detection unit 2 comprises flip-flops FFs 21 and 22 and Exclusive OR circuits 23 and 24 for providing a comparison signal. The digital PLL unit 3 comprises a sequential filter 35, an oscillator 31, a pulse control circuit 32, a first divider 33, and a second divider 34 for generating clock signals.

With respect to claim 47, the A/D converters 57 and 58 along or with the combination of the mixers 51 and 52, the filters 55 and 56, the operation circuit 59, the discriminators 60 and 61, and the P/S converter 62 correspond to the identifying circuit for identifying the IF signal; the bit time recovery circuit 1 corresponds to the clock regenerating circuit, which comprises the phase comparison result detection unit 2 and the digital PLL unit 3; the phase comparison result detection unit 2 corresponds to the clock phase detecting unit; the filter 35 corresponds to the loop filter unit; and the oscillator 31, the pulse control 32, and the dividers 33 and 34 correspond to the oscillator unit.

14. Claim 47 is rejected under 35 U.S.C. 102(e) as being anticipated by Kobayashi (previously cited).

Kobayashi (U.S. Patent No. 5,535,252) discloses a clock synchronization circuit in Fig. 2 for use in a base-band demodulator of communication equipment of a digital modulation type.

In Fig. 2, the base-band demodulator 4 comprises A/D converters 41 and 42 for converting analog signals a and b into digital signals c and d; a delay detector 43 for detecting the digital signals to provide detected signals e and f; a judger circuit 44 for judging the detected signals to provide a judged signal g; a PLL 40 for providing clock signals; a limiter 45; a band pass filter 46; a phase error detector 47; a clock reproducer 48; and a frequency divider 49.

With respect to claim 47, the A/D converters 41 and 42 correspond to the identifying circuit for identifying the IF signal a and b; the PLL 40 and the reproducer 48

correspond to the loop filter unit and the oscillating unit (note it is well known in the art that the PLL 40 includes at least a loop filter and an oscillator); and the clock reproducer 48 corresponds to the clock phase detecting unit.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

References Schneider (U.S. Patent No. 5,216,554) and Tuttle et al. (U.S. Patent No. 5,796,535) are related to a phase demodulator circuit having a carrier phase synchronization circuit for providing a controlled clock signal to an identifying circuit of the phase demodulator circuit.

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Young Tse** whose telephone number is **(703) 305-4736**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Jay Patel**, can be reached at **(703) 308-7728**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

P.O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Young T. Tse
Primary Examiner
7/24/04